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09/614,407	07/12/2000	Bo Zheng	AMAT/4471/CALB/COPPER/SB	1903

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EXAMINER	
MUTSCHLER, BRIAN L	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

mk-20

Office Action Summary	Application No.	Applicant(s)	
	09/614,407	ZHENG ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *86-101* is/are allowed.

6)☒ Claim(s) *32-84* is/are rejected.

7)☒ Claim(s) *85* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Comments

1. The indicated allowability of claims 32-84 is withdrawn in view of the newly discovered reference(s) to Reid et al. (US 2001/0015321 A1), Chung et al. (U.S. Pat. No. 6,409,903 B1) Lopatin et al. (U.S. Pat. No. 6,340,611 B1) and Landau (WO 99/54527 A2). Rejections based on the newly cited reference(s) follow.

2. The rejections of claims 86, 87, 89, 90 and 96 under 35 U.S.C. 112, first paragraph, have been overcome by Applicant's amendment, which replaced the new matter with limitations supported by the specification.

3. The rejection of claims 85-92 under 35 U.S.C. 103 over Taylor et al. in view of Tsai et al. has been overcome by Applicant's amendment. The prior art of record neither teaches nor suggests increasing or ramping the current while the substrate is being immersed in the electrolyte.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

a. Figure 3 does not show the electric current ramp designated by the reference sign **319** (see page 17, line 13).

b. Figures 6A to 6F do not show the metal deposited layer designated by the reference sign **604** (see page 14, line 33).

c. Figures 6E and 6F do not show the spaces designated by the reference sign **622** (see page 20, lines 10 and 21).

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

a. The reference signs **24**, **86** and **82** shown in Figure 1 are not identified in the specification.

b. The reference sign **200** shown in Figure 2A is not identified in the specification. The same reference sign also appears in Figures 2B and 6A-6F.

c. The reference sign **530** shown in Figure 5 is not identified in the specification.

6. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claim 85 is objected to because of the following informalities:

a. In claim 85 at lines 9-10, please delete "[, the plating voltage being higher than the initial portion of the first biasing voltage]".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 32, 55-59, 61-67 and 78-84 are rejected under 35 U.S.C. 102(a) as being anticipated by WO 99/54527 A2, herein referred to as WO '527.

Regarding claims 32, 67 and 78, WO '527 discloses a method and system for electroplating substrates comprising forming a seed layer on the substrate (page 4, first full paragraph) followed by electroplating copper on the seed layer by applying different currents (see "Operating Conditions" beginning on page 22). A voltage is applied to the substrate before the substrate is introduced to the electrolyte to prevent the seed layer from being dissolved by the electrolyte, or alternatively, a current is applied as the substrate comes into contact with the electrolyte (page 24, fourth paragraph). At the beginning of the plating cycle, a high current density strike is applied (page 24, third paragraph). To fill the vias and trenches, a pulsed cycle comprising deposition current densities and dissolution current densities is applied (page 23, first full paragraph).

While WO '527 discloses the application of voltages, currents and current densities, it is noted that these values are all related. According to Ohm's law, the voltage, V, is equal to the product of the resistance, R, and the current, i: V=iR. Since the resistance is a property of the substrate and does not change when the above method switches from a voltage or current while immersing the substrate, the voltage is directly proportional to the current, i.e., a change in the current results in a proportional change in the voltage, and likewise, a change in the voltage is accompanied by a proportional change in the current.

Therefore, WO '527 teaches a means for providing a seed layer and means for applying a voltage, wherein the means for applying the voltage is capable of performing the intended functions, such as applying a voltage while the substrate is immersed, applying higher or lower voltages, and applying pulsed voltages.

Regarding claims 55-59, WO '527 discloses the use of reverse currents in the deposition/dissolution cycle to provide deposition and dissolution of the electroplated layer (page 23, first full paragraph).

Regarding claims 61 and 62, WO '527 discloses, "conventional copper plating electrolyte includes a high sulfuric acid concentration" (page 25, third paragraph).

Regarding claims 63-66, the applied currents of WO '527 are used for deposition of copper, which would limit etching (pages 22-25). Furthermore, the second applied current density has a higher current density than the first current density, which is about 5 mA/cm^2, and would therefore have a higher deposition than the deposition caused by the first deposition (page 23, second and third paragraphs).

Regarding claims 67, 83 and 84, WO '527 discloses the use of reverse currents in the deposition/dissolution cycle to provide deposition and dissolution of the electroplated layer (page 23, first full paragraph).

Regarding the limitations recited in claims 79-81, each of the deposition voltages applied in the process of WO '527 is capable of depositing metal on the seed layer, and as a deposition voltage, is therefore also limiting etching, which is the reverse of deposition (see pages 22-25).

Regarding claim 82, the means for applying the different voltages is also capable of applying a third voltage higher or lower than another of the voltages.

Since WO '527 teaches all of the limitations recited in the instant claims, the reference is deemed to be anticipatory.

10. Claims 78-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Reid et al. (US 2001/0015321 A1).

Reid et al. disclose an electroplating process for filling features of integrated circuit devices, wherein the process discloses the use of a "patterned substrate onto which a seed layer has been deposited" (page 1, par. [0009]). In order to have a substrate "onto which a seed layer has been deposited", means for depositing the seed layer on the substrate are inherently required. In the method of Reid et al., four different plating phases are identified. In the first phase, a small current density is applied while the substrate is being immersed in the substrate to avoid corrosion of the seed layer (page 3, par. [0021]). In the second phase, a second current density is applied to the

substrate (page 3, par. [0025]). The current density used in the second phase can comprise ramped or constant current densities, or the current density can comprise a pulse cycle having anodic and cathodic pulses (page 3, par. [0025]). The third phase comprises a third current density that is typically a ramped current (page 4, par. [0028]). The fourth phase uses a fourth current density that can also be ramped (page 4, par. [0029]).

As explained above in section 9, the voltage and current are related to each other through Ohm's law. Current density is equal to the current divided by the area of the substrate and is used because it provides a more illustrative description of the plating process than a recitation of the current alone because it is related to the deposition rate of the plated material. Since Reid et al. disclose the use of different current densities, which inherently require a means for providing the current densities, the voltages also differ as evidenced by Ohm's law.

Regarding the limitations recited in claims 79-81, each of the deposition voltages applied in the process of Reid et al. is capable of depositing metal on the seed layer, and as a deposition voltage, is therefore also limiting etching, which is the reverse of deposition (see paragraphs [0021] to [0029]).

Regarding claim 82, the means for applying the different voltages is also capable of applying a third voltage higher or lower than another of the voltages.

Regarding claims 83 and 84, Reid et al. disclose the use of both anodic and cathodic currents in the pulse cycle to provide deposition and dissolution of the electroplated layer (page 3, par. [0025]).

Since Reid et al. teach all of the limitations recited in the instant claims, the reference is deemed to be anticipatory.

Reid et al. is a continuation-in-part of U.S. Application No. 09/410,170, which is a non-provisional of provisional Application No. 60/105,699. The parent application has been carefully reviewed and the subject matter relied upon for the rejection above is fully supported.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 33-54, 60 and 68-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 99/54527, optionally in view of Chung et al. (U.S. Pat. No. 6,409,903).

WO '527 teaches a method for electroplating copper on a seed layer having the limitations recited in claims 32, 55-59, 61-67 and 78-84 of the instant invention as explained above in section 9.

Regarding claims 33, 35, 45, 46 and 68, the current density of applied in the high current density strike ranges from about 100 mA/cm^2 to about 1000 mA/cm^2 and the current density of the deposition cycle ranges from about 5 mA/cm^2 to about 40 mA/cm^2 (pages 23-24). Because the current is proportional to the voltage, the high current

density strike (equivalent to the second biasing voltage) is higher than the subsequent applied voltages (third and pulsed biasing voltages). Furthermore, assuming a circular substrate, which is implied by the use of the term "diameter" in claims 44-46, the claimed limitation recites the equivalent plating current density of about 40 mA/cm^2, which is within the range taught by WO '527.

Regarding claims 50, 51, 52, 54, 76 and 77, WO '527 claims an embodiment wherein the pulsed current is applied ranging from 1.1 seconds to 340 seconds or more, depending upon the number of cycles (see claim 31 on page 33).

Regarding claim 60, WO '527 discloses the use of reverse currents in the deposition/dissolution cycle to provide deposition and dissolution of the electroplated layer (page 23, first full paragraph).

The method of WO '527 differs from the instant invention because WO '527 does not disclose the following:

a. A third biasing voltage, as recited in claims 33-35, 45, 46 and 68.

b. The operating conditions (time, voltage, current, number of cycles), as recited in claims 34-54, 60 and 69-77.

Regarding the third biasing voltage recited in claims 33-35, 45, 46 and 68, the third biasing voltage is not distinguished over the pulsed biasing voltage. Since the third biasing voltage and the pulsed biasing voltage are both biasing voltages, one skilled in the art would recognize that the limitations recited for the third biasing voltage are included in the pulsed biasing voltage as taught by WO '527 because the third biasing

voltage could be considered the first of the pulses, or since WO '527 discloses that a single pulse could be used (see page 23, first full paragraph, third sentence), as defined by the use of a single dissolution pulse, the third biasing voltage could be either the deposition current preceding the pulse or the deposition current following the pulse.

Regarding the operating conditions (i.e., time, voltage, current, number of cycles) recited in claims 34-54, 60 and 69-77, the operating conditions are result effective variables. Based on the teachings of WO '527, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the operating conditions recited in the instant claims because the operating conditions are commensurate in scope, e.g., current and voltage (based on the disclosed current densities of both WO '527), with the teachings of WO '527.

Additionally, Chung et al. disclose a method for electroplating on semiconductor wafers wherein the method utilizes potentiostatic or galvanostatic plating control. Chung et al. also disclose the use of ramped or stepped waveform profiles comprising a plurality of biasing voltages to plate uniform layers (figs. 3 and 4; col. 2, line 1 to col. col. 3, line 14). The substrates are 200 mm in diameter and use current densities in the range of 30 mA/cm^2 (col. 5, lines 18-21). Furthermore, Chung et al. teach, "[The plating times] will be determined based on the wafer to be plated and the electrolyte used and operating temperature" and that the operating voltage is calculated based on the particular substrate and electrolytic plating cell (col. 7, lines 18-25).

Optionally, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the operating conditions used in the

method of WO '527 to use the claimed operating conditions because Chung et al. teach that the operating conditions must be calculated for each substrate based upon the electrolyte, the operating temperature, the electrolytic cell, and the substrate itself.

13. Claims 67 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al. (US 2001/0015321 A1) in view of Lopatin et al. (U.S. Pat. No. 6,340,633).

Reid et al. disclose an electroplating process for filling features of integrated circuit devices, wherein the process discloses the use of a "patterned substrate onto which a seed layer has been deposited" (page 1, par. [0009]). In order to have a substrate "onto which a seed layer has been deposited", means for depositing the seed layer on the substrate are inherently required. In the method of Reid et al., four different plating phases are identified. In the first phase, a small current density is applied while the substrate is being immersed in the substrate to avoid corrosion of the seed layer (page 3, par. [0021]). In the second phase, a second current density is applied to the substrate (page 3, par. [0025]). The current density used in the second phase can comprise ramped or constant current densities, or the current density can comprise a pulse cycle having anodic and cathodic pulses (page 3, par. [0025]). The third phase comprises a third current density that is typically a ramped current (page 4, par. [0028]). The fourth phase uses a fourth current density that can also be ramped (page 4, par. [0029]). In the method of Reid et al. the first phase is the "entry phase", which provides protection against the corrosion of the seed layer; the second phase is the "initiation

phase", which is used to nucleate and grow a "relatively thin", conformal film on the seed layer; and the third and fourth phases are used to fill the features uniformly using a ramped current density (see paragraphs [0021] to [0029]). In the method of Reid et al., the current provided in the "entry phase" corresponds to the first biasing voltage, the current density provided in the "initiation phase" corresponds to the second biasing voltage, and the third and fourth phases correspond to the plating provided by the pulsed biasing voltage in the instant claim.

As explained above in section 9, the voltage and current are related to each other through Ohm's law. Current density is equal to the current divided by the area of the substrate and is used because it provides a more illustrative description of the plating process than a recitation of the current alone because it is related to the deposition rate of the plated material. Since Reid et al. disclose the use of different current densities, which inherently require a means for providing the current densities, the voltages also differ as evidenced by Ohm's law.

The method of Reid et al. differs from the instant invention because Reid et al. do not disclose the following:

a. Applying a pulsed biasing voltage configured to apply a positive plating current and a negative deplating current, as recited in claim 67.

b. Applying a third biasing voltage, as recited in claim 68.

Regarding claim 67, Lopatin et al. disclose a method for plating features in semiconductors comprising the use of a ramped pulse current having positive plating currents and negative plating currents (fig. 4; col. 2, lines 58-63). Lopatin et al. teach,

"[U]sing a ramped forward pulse current for the electroplating process... speeds up the overall manufacturing process and deposits a fine grain structure conductive layer which increases electromigration resistance" (col. 2, lines 58-63).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the plating phases (third and fourth phases) of Reid et al. to use a pulsed current as taught by Lopatin et al. because the pulsed current process of Lopatin et al. increases electromigration resistance and speeds up the overall manufacturing process.

Regarding the third biasing voltage recited in claim 68, the third biasing voltage is not distinguished over the pulsed biasing voltage. Since the third biasing voltage and the pulsed biasing voltage are both biasing voltages, one skilled in the art would recognize that the limitations recited for the third biasing voltage are included in the pulsed biasing voltage as described above by Reid et al. and Lopatin et al. because the third biasing voltage could be considered any one of the pulses in the plating process.

14. Claims 69-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reid et al. (US 2001/0015321 A1) in view of Lopatin et al. (U.S. Pat. No. 6,340,633), as applied above to claims 67 and 68, and further in view of Chung et al. (U.S. Pat. No. 6,409,903).

Reid et al. and Lopatin et al. describe a method having the limitations recited in claims 67 and 68 of the instant invention, as explained above in section 13.

The method described by Reid et al. and Lopatin et al. differs from the instant invention because they do not disclose the operating conditions (time, voltage, current, number of cycles), as recited in claims 69-77.

Chung et al. disclose a method for electroplating on semiconductor wafers wherein the method utilizes potentiostatic or galvanostatic plating control. Chung et al. also disclose the use of ramped or stepped waveform profiles comprising a plurality of biasing voltages to plate uniform layers (figs. 3 and 4; col. 2, line 1 to col. col. 3, line 14). The substrates are 200 mm in diameter and use current densities in the range of 30 mA/cm^2 (col. 5, lines 18-21). Furthermore, Chung et al. teach, "[The plating times] will be determined based on the wafer to be plated and the electrolyte used and operating temperature" and that the operating voltage is calculated based on the particular substrate and electrolytic plating cell (col. 7, lines 18-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the operating conditions used in the method described by Reid et al. and Lopatin et al. to use the claimed operating conditions because Chung et al. teach that the operating conditions must be calculated for each substrate based upon the electrolyte, the operating temperature, the electrolytic cell, and the substrate itself.

Response to Arguments

15. Applicant's arguments regarding claims 85-92 are moot because the amendments have overcome the rejections.

Allowable Subject Matter

16. The following is a statement of reasons for the indication of allowable subject matter: Claims 85-101 are distinguished over the prior art because they describe a method for electroplating comprising the step of immersing the substrate in an electrolyte while ramping or increasing the current. This feature is neither taught nor suggested in the prior art of record. Both WO '527 and Reid et al. disclose the use of a current being applied to the substrate as it is being immersed in the electrolyte, but neither reference discloses changing the current while it is being immersed. Increasing or ramping the current while immersing the substrate is a useful advantage because increasing the current while immersing the substrate can help maintain a more constant current density while the substrate is immersed. As more of the substrate is immersed, and consequently more of its area is contacted by the electrolyte, the current density will not decrease if the current is increased. This can be important because the current density is related to the deposition and/or dissolution rate. A current sufficient for preventing the dissolution of the seed layer when the first portion of the substrate contacts the electrolyte may not be adequate to prevent the etching of the seed layer as more of the substrate is immersed. The instant invention provides a means for increasing the current, which could improve the prevention of seed layer etching.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 6,440,291 (Henri et al.) and U.S. Pat. No. 4,891,106 (Domnikov) disclose methods for providing a voltage to a substrate while the substrate is immersed in an electrolyte. U.S. Pat. No. 6,432,821 (Dubin et al.) discloses several complex waveforms for copper electroplating comprising stepped increases and pulse plating cycles.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (703) 305-0180. The examiner can normally be reached on Monday-Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (703) 308-3322. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

blm
June 4, 2003